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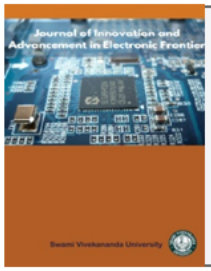

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Performance Comparison of NOT Gate Implementations in GPDK45 and GPDK180 Technologies: A Virtuoso-Based Study

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Abstract

This study presents a comparative analysis of NOT gate performance using two different process design kits (PDKs): GPDK45 and GPDK180. The research utilizes Cadence Virtuoso software to design and simulate the NOT gate, evaluating key performance metrics such as propagation delay, power consumption, and area. The methodology involves creating the schematic and layout for the NOT gate using both GPDK45 and GPDK180, followed by generating symbols and constructing circuits to observe the gate's behavior under various conditions. The analysis includes input-output characteristics, DC response, and transient analysis to determine the gate's time delay and overall efficiency. Results show significant performance differences, with GPDK45 technology offering superior speed and reduced area at the expense of higher power consumption compared to GPDK180. These findings highlight the trade-offs in selecting a technology node for specific applications, providing valuable insights for designers aiming to optimize digital circuits in advanced semiconductor technologies. This research contributes to the ongoing efforts to scale down semiconductor devices while maintaining high performance and energy efficiency, serving as a reference for engineers and researchers working on digital circuit design.

Keywords: *Circuit Simulation, GPDKxx, Cadence Virtuoso, IC designing, Layout designing*

1. Introduction

The relentless pursuit of smaller, faster, and more energy-efficient semiconductor devices has driven the evolution of integrated circuit (IC) technology through multiple generations [1]. As technology continues to scale down, each new process node introduces distinct advantages and challenges, significantly impacting the design and performance of digital circuits. Among the essential components of digital logic, the NOT gate (or inverter) holds a critical role [2], frequently serving as a benchmark for assessing the performance of various process technologies [2, 3]. This paper conducts a comparative analysis of the NOT gate using two process design kits (PDKs):

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GPDK45 and GPDK180. GPDK45, based on a 45nm technology node (Badiger & Iyer, 2024), representsa more advanced and miniaturized process compared to GPDK180, which operates on a 180nm technology node. The comparison between these two nodes [4] is especially pertinent as designers must weigh the benefits of reduced area and increased speed offered by smaller nodes like GPDK45 against the potential for lower power consumption and simpler fabrication processes associated with larger nodes like GPDK180.

This study utilizes Cadence Virtuoso [5], a prominent electronic design automation (EDA) tool, to design, simulate, and evaluate the performance of the NOT gate in both technologies. The NOT gate's schematic, symbol, layout, and corresponding input-output characteristics [5, 6] are carefully developed and analyzed to assess critical performance metrics such as propagation delay, power dissipation, and area efficiency. By examining the DC response and transient characteristics, this research offers a thorough understanding of how scaling affects the performance of fundamental logic gates. The findings of this study will provide valuable insights for circuit designers, assisting them in making informed decisions when selecting the appropriate technology node for specific applications. Additionally, this research contributes to the ongoing discussion about the trade-offs involved in semiconductor scaling, especially as the industry nears the physical and economic boundaries of Moore's Law.

2. Overview

Schematic Drawing

The NOT gate, commonly known as an inverter, is a fundamental component in digital electronics. It operates by reversing the input signal—when the input is high (logic 1), the output becomes low (logic 0), and when the input is low (logic 0), the output turns high (logic 1). This basic functionality plays a crucial role in digital circuit design, making the NOT gate an essential building block. To design a NOT gate schematic in Cadence Virtuoso, as described in [7, 8] begin by creating a new library to store the design files. Within this library, define a new cell, such as "NOT_gate_schematic" or any preferred name. Open the schematic editor and select the necessary components, typically an NMOS and a PMOS transistor, which together form the CMOS-based inverter.

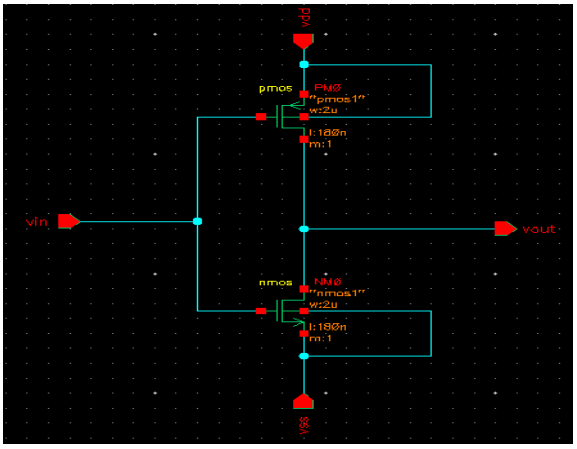

Fig. 1 Schematic Drawing of NOT Gate

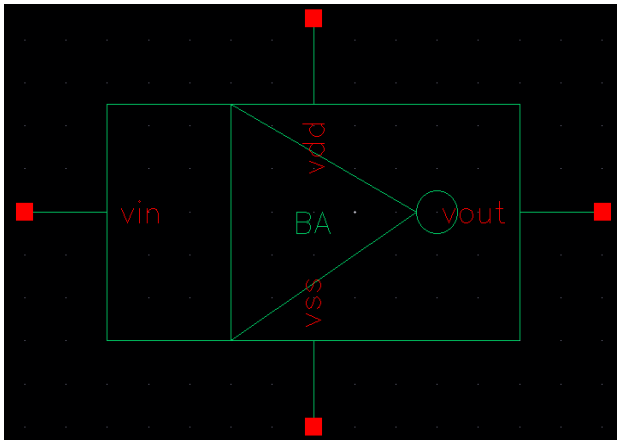

Fig. 2 Symbol of NOT Gate

First, place the PMOS transistor so that its drain connects to the output node and its source links to the supply voltage (VDD). Similarly, position the NMOS transistor with its drain attached to the output node and its source connected to ground (GND). The gates of both transistors should be tied together to serve as the input of the NOT gate. This common gate connection ensures that both transistors receive the same input signal. After placing the transistors, use wires to establish the necessary connections. The output is taken from the junction of the PMOS and NMOS drains. Ensuring correct wiring and connections is crucial for the schematic to function as intended. The generated schematic (Fig. 1) visually represents the arrangement of PMOS and NMOS transistors in a CMOS

inverter, demonstrating how these transistors are interconnected to achieve logic inversion [2, 11]. This schematic highlights the essential structure and connectivity required for the NOT gate to function correctly.

Operation of the NOT Gate

The functionality of the NOT gate [12] relies on the complementary switching behavior of PMOS and NMOS transistors:

1. **When the input is low (logic 0):** The NMOS transistor remains off, while the PMOS transistor turns on. This allows the output to be pulled high, producing a logic 1 at the output.
2. **When the input is high (logic 1):** The NMOS transistor turns on, and the PMOS transistor switches off. As a result, the output is pulled low, generating a logic 0.

This complementary operation ensures that the output always reflects the inverse of the input signal, thereby fulfilling the logic inversion function of the NOT gate.

Symbol Creation

In digital circuit design, generating a symbolic representation of the NOT gate is an essential step, as it simplifies its integration into more complex circuits. The symbol offers a standardized and easily recognizable depiction of the NOT gate, streamlining its use in various designs [7, 14]. This eliminates the need to redraw the internal circuit structure each time, making circuit development more efficient. After finalizing the schematic, the next step involves generating the symbol for the NOT gate. To do this, open the Symbol Editor in Virtuoso by selecting the "Create Cellview" option and choosing "Symbol" as the view type. This action will launch a blank workspace where the symbolic representation of the NOT gate can be designed. Typically, a NOT gate is illustrated as a triangle pointing to the right, with a small circle at its output to indicate the inversion function. Using the drawing tools available in the Symbol Editor, begin by sketching a triangle to form the main body of the NOT gate. Then, place a small circle at the output end of the triangle to signify the logic inversion. This graphical representation is a widely accepted standard for NOT gates in digital circuit design. Once the basic shape is completed, the next step is to define the input and output pins. Position an input pin on the left side of the triangle and label it as "In" or another suitable name to represent the gate's input terminal. Similarly, place an output pin on the right side of the triangle and label it as "Out" to denote the gate's output terminal. Ensure that these pins are properly aligned with the symbol and accurately correspond to the input and output terminals in the underlying schematic.

After positioning the pins, refine the symbol by adjusting its properties. This includes assigning appropriate labels, modifying pin names if necessary, and ensuring that the overall appearance aligns with standard circuit design conventions. Once the symbol has been fully designed, save the work and verify that it correctly corresponds to the schematic. This involves ensuring that the input and output pins on the symbol are properly mapped to their respective nodes in the schematic representation. The finalized symbol (Fig. 2) offers a clear and intuitive depiction of the NOT gate, facilitating its use in future circuit designs. By providing an abstracted version of the detailed schematic, the symbol enables circuit designers to focus on higher-level functionality without being encumbered by intricate low-level details.

3. Design Implementation

After developing both the schematic and symbol for the NOT gate, the next step is to incorporate the symbol into a complete circuit. This stage involves integrating the NOT gate into a broader circuit environment, allowing it to interact with other components and operate under different input conditions [11- 15]. The use of a symbol streamlines this process by enabling the designer to concentrate on overall circuit functionality without delving into the internal workings of the NOT gate.

Circuit Design in Virtuoso

To construct a circuit utilizing the NOT gate symbol in Cadence Virtuoso, begin by creating a new schematic cell within the project library. Assign an appropriate name to this cell, such as "NOT_gate_circuit." Once the new cell is established, open the Schematic Editor and place the previously designed NOT gate symbol onto the schematic workspace. This symbol encapsulates the transistor-level details of the NOT gate, simplifying circuit integration.

Next, establish the power connections by incorporating VDD and GND pins into the circuit. These power connections are essential for operating the internal transistors within the NOT gate. Specifically, the VDD pin should be connected to the source terminal of the PMOS transistor, while the GND pin should be linked to the source terminal of the NMOS transistor. The NOT gate symbol implicitly manages these connections, ensuring correct functionality. After setting up the power connections, introduce an input signal by placing an appropriate input source, such as a pulse generator or a DC voltage source, within the schematic. This input source is responsible for supplying the required signal to the NOT gate, with its output connected to the input pin ("In") of the NOT gate symbol. This connection enables the gate to perform its logic inversion operation based on the applied signal. Finally, integrate an output load, such as a capacitor or resistor, to the output terminal of the NOT gate. This load helps simulate realistic operating conditions and is connected to the output pin ("Out") of the NOT gate symbol. The output signal will reflect the inverted version of the input, ensuring the expected logic operation. Additionally, any necessary measurement probes should be placed at the output to facilitate signal analysis during simulations.

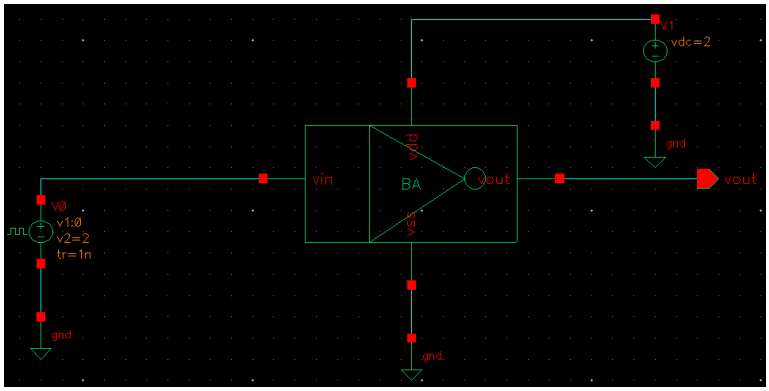

Fig. 3 Circuit Design of NOT Gate

The final circuit design, as illustrated in Fig. 3, effectively employs the NOT gate symbol to construct a fully functional digital circuit. This phase of circuit design allows for an in-depth analysis of the NOT gate's performance under practical conditions, showcasing its response to real-world input signals and circuit loads.

Layout Design in Virtuoso

The layout design plays a crucial role in the integrated circuit (IC) design process, as it involves converting the schematic of the NOT gate into a physical representation that can be manufactured on a silicon wafer [9, 10]. This step is essential because it defines the precise geometric arrangement of transistors, interconnections, and other circuit elements, ensuring that the design adheres to the required performance specifications and area constraints. In this section, we will explore the layout design process for the NOT gate, focusing on implementations using both GPDK45 and GPDK180 technologies. These layout designs, illustrated in Fig. 4 and Fig. 5, demonstrate how different process technologies impact the physical realization of the circuit. By carefully planning the layout, designers can optimize the circuit’s efficiency, minimize parasitic effects, and ensure proper functionality in fabrication.

The process of designing the layout for the NOT gate in Cadence Virtuoso involves several key steps, ensuring that the physical implementation accurately reflects the schematic while adhering to design constraints.

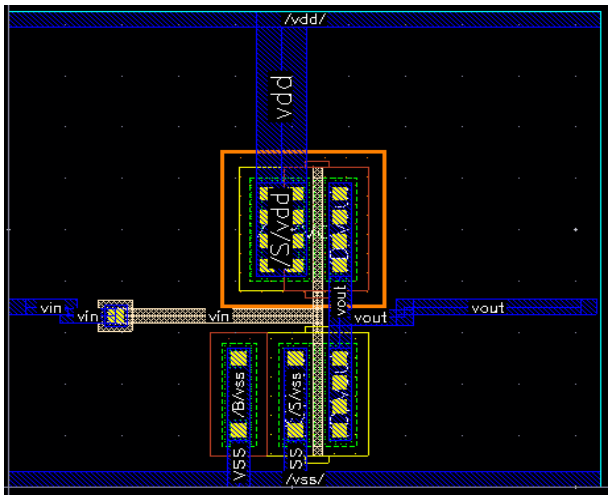

Fig. 4 Layout Design in GPDK180

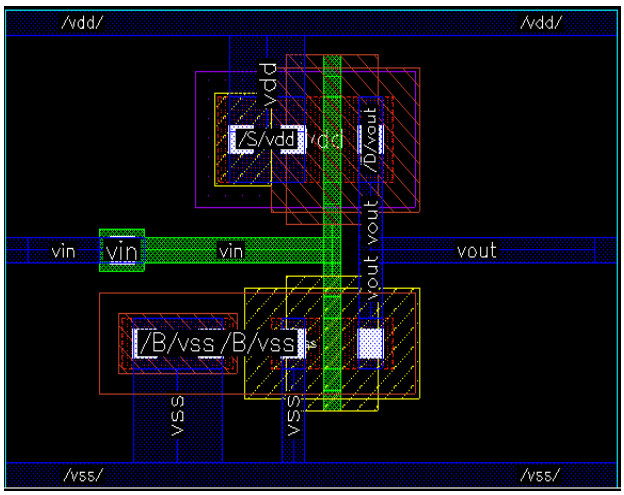

Fig. 5 Layout Design in GPDK45

The following steps outline the typical procedure:

1. Initializing the Layout Editor: Begin by launching the Layout Editor in Virtuoso and creating a new layout view that corresponds to the NOT gate schematic. This layout view serves as the workspace for arranging and connecting the various layers that form the CMOS transistors.
2. Placing the Transistors:
    a. For both **GPDK45** and **GPDK180**, position the PMOS and NMOS transistors according to the design rules specified for each technology. The placement should be optimized to minimize the occupied area while ensuring efficient routing of interconnections.
    b. **GPDK45 Layout (Fig. 4):** In the 45nm technology node, transistors are significantly smaller, allowing for a highly compact layout. The spacing between the source, drain, and gate regions is minimized, resulting in a denser configuration. While this reduced feature size enables better scaling and improved circuit performance, it demands precise alignment and strict adherence to design rules to mitigate parasitic effects.
    c. **GPDK180 Layout (Fig. 5):** In contrast, the 180nm technology node features larger transistors, leading to a more spacious layout. The increased separation between components simplifies the routing process but requires more area. This technology is generally more robust against variations and manufacturing defects, making it easier to implement, though it is less efficient in terms of density.
3. Routing the Interconnections:
    a. Establish electrical connections between the source, drain, and gate terminals of the transistors using appropriate metal layers.
    b. **In GPDK45**, the reduced feature sizes lead to narrower interconnects, requiring advanced routing techniques to prevent signal interference and maintain circuit performance. Due to the limited space, multiple metal layers are often necessary to achieve effective signal routing while minimizing resistance and capacitance.
    c. **In GPDK180**, the larger interconnects facilitate easier routing but may introduce higher parasitic capacitance, which can impact circuit speed. However, the layout process is generally more manageable, with less stringent design constraints and more relaxed routing requirements.

Differences Between GPDK45 and GPDK180 Layouts

The key distinctions between the layouts designed for GPDK45 and GPDK180 technologies primarily revolve around their scale, density, and complexity. One major difference lies in the **density** of the layout. GPDK45 enables a much denser design due to its smaller transistor sizes and narrower interconnects. This high-density layout allows circuits to occupy a smaller area, making it particularly advantageous for high-performance applications where minimizing space is critical. On the other hand, GPDK180 features larger components, resulting in a more spread-out layout with reduced density. Another important factor is **routing complexity**. The GPDK45 layout demands advanced routing strategies to accommodate the narrower metal layers and closely packed components. This often increases design complexity and necessitates the use of multiple metal layers to ensure proper connectivity while avoiding signal interference. In contrast, GPDK180 provides wider interconnects and greater spacing between components, making routing more straightforward. However, this comes at the expense of increased parasitic capacitance and a larger overall circuit footprint. **Design rules** also differ significantly between these two technologies. GPDK45 enforces much stricter design constraints due to its smaller feature sizes, requiring precise alignment and high-resolution lithography techniques to ensure accuracy [5]. GPDK180, in comparison, follows more relaxed design rules, allowing for greater tolerance to manufacturing variations. However, this trade-off means that GPDK180 does not achieve the same level of miniaturization and performance optimization as GPDK45.

4. Results and Discussion

This section provides a comprehensive comparison of the NOT gate's performance when implemented using GPDK45 and GPDK180 technologies. The analysis focuses on key performance metrics such as the output waveform, DC response, and propagation delay, all of which are essential for assessing the efficiency and effectiveness of the gate across different technology nodes. Figures 6 and 7 illustrate the output graph and DC response, respectively.

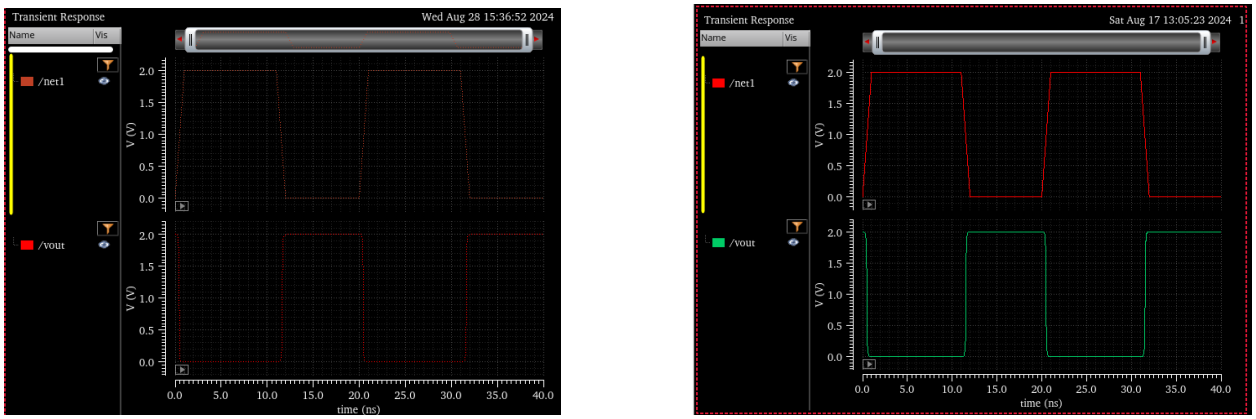

Fig. 6 Transient output waveform for GPDK180 (left) and GPDK45 (right)

The output waveform analysis offers valuable insights into the behavior of the NOT gate when responding to an input signal in both GPDK45 and GPDK180 technologies. The waveform reflects the gate's ability to invert the input and transition between logic states. In the case of **GPDK45**, the output waveform exhibits a much sharper transition between logic levels. The gate switches rapidly from high to low and vice versa, demonstrating the high-speed performance characteristic of the 45nm node. The rise and fall times are significantly shorter compared to GPDK180, highlighting the superior switching speed and higher frequency capability of this technology. This fast response is particularly beneficial for high-performance applications where precise timing is a critical requirement. On the other hand, the **GPDK180** output waveform reveals a slower transition between logic levels. The rise and fall times are noticeably longer, which reflects the inherently reduced speed of the 180nm technology. This slower

switching behavior can result in less precise timing within circuits, making GPDK180 more suitable for applications where speed is not the primary focus.

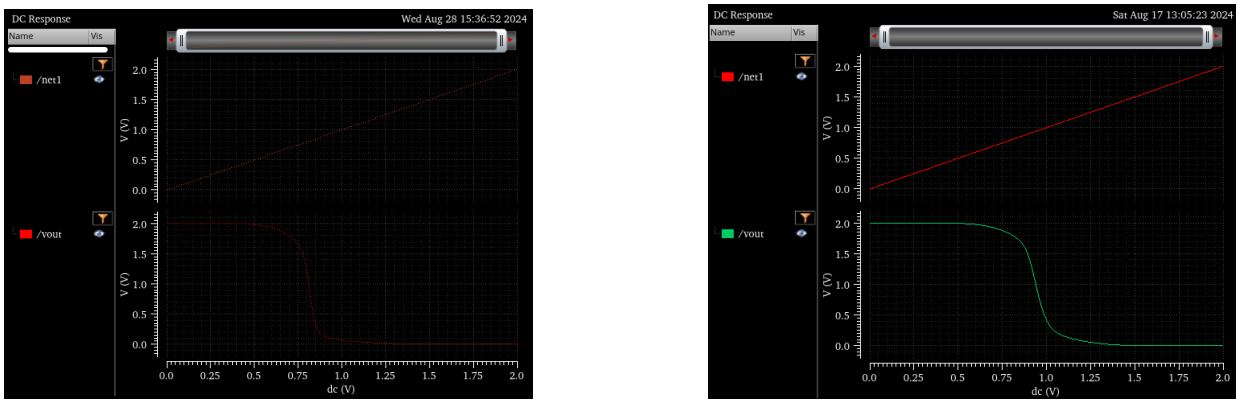

Fig. 7 DC Response waveform for gpdk180 (left) and gpdk45 (right)

Instead, it is better suited for scenarios where power efficiency and robustness take precedence. The contrast between these two technologies highlights the trade-offs involved in choosing between them. The sharper transitions observed in GPDK45 make it well-suited for high-speed digital circuits, where performance is paramount. In contrast, the more gradual transitions seen in GPDK180 may contribute to lower power consumption, albeit at the expense of speed.

DC Response Analysis

The DC response of the NOT gate, as illustrated in Fig. 7, demonstrates the relationship between the input voltage and the output voltage, offering a static representation of the gate's transfer characteristics. This analysis provides insights into how the output behaves as the input transitions across different voltage levels. In GPDK45, the DC response exhibits a steep transition around the threshold voltage. This sharp slope indicates a strong and rapid switching capability, with the output voltage quickly reaching its maximum or minimum value as soon as the input surpasses the threshold. The pronounced sharpness of this transition suggests that GPDK45 has a narrower threshold voltage window, which enables faster and more precise operation. The ability to switch swiftly between logic levels makes this technology particularly well-suited for high-speed digital applications where quick response times are essential. Conversely, the DC response in GPDK180 displays a more gradual transition. The slope around the threshold voltage is less steep, signifying that the output voltage changes more slowly when the input crosses the threshold. This behavior can be advantageous in terms of noise margins, as it makes the gate less susceptible to minor fluctuations in the input signal. However, the slower response also means that the gate takes longer to switch between logic states, aligning with the overall reduced speed observed in the output waveform. This comparison highlights the key differences between the two technology nodes. GPDK45 provides a sharper and more defined switching behavior, making it ideal for applications that demand rapid and accurate logic operations. On the other hand, GPDK180 offers a more robust and stable response, making it a preferable choice for environments where lower power consumption and improved noise tolerance are prioritized over switching speed.

Propagation Delay Comparison

Propagation delay is a crucial parameter that quantifies the time required for a signal to pass through the NOT gate, directly influencing the overall speed of a digital circuit. This factor plays a significant role in determining the efficiency and performance of different technology nodes. In GPDK45, the propagation delay is considerably lower, typically ranging between 10 to 15 picoseconds. This minimal delay results from the smaller transistor dimensions and faster switching speeds characteristic of the 45nm technology. The reduced capacitance and

resistance in the interconnects further contribute to the rapid signal transmission, making GPDK45 an excellent choice for high-speed and high-frequency applications where precise timing is essential. The ability to switch states quickly ensures that this technology is well-suited for modern computing systems requiring optimal performance. On the other hand, GPDK180 exhibits a significantly higher propagation delay, generally around 60 to 70 picoseconds. The larger transistor sizes inherent in this 180nm technology lead to increased parasitic capacitance and resistance, which ultimately slow down signal propagation. Although this longer delay makes GPDK180 less suitable for high-speed applications, it presents advantages in low-power designs where slower operation is acceptable. The higher delay may also contribute to improved noise tolerance, making GPDK180 a more viable option for circuits prioritizing stability and power efficiency over speed.

The notable disparity in propagation delays highlights the trade-offs between these two technology nodes. While GPDK45 excels in terms of speed, making it the preferred choice for high-performance computing, GPDK180, with its longer delay, may be more beneficial for applications that prioritize power efficiency, cost-effectiveness, and noise resilience.

6. Conclusion and Future Work

The comparison between GPDK45 and GPDK180 technologies highlights a distinct trade-off among speed, power consumption, and design complexity. GPDK45 demonstrates superior performance across multiple metrics, including sharper output transitions, a steeper DC response, and significantly lower propagation delays. These characteristics make it highly suitable for high-speed and high-performance applications where rapid signal transitions and precise timing are essential. The ability to switch states quickly ensures that GPDK45 is well-optimized for computing systems and circuits that demand maximum efficiency and responsiveness. In contrast, GPDK180 exhibits more gradual transitions and a higher propagation delay, making it less ideal for applications requiring extreme speed. However, this technology offers advantages in areas where power efficiency, robustness, and simplified design rules are prioritized. The larger feature sizes and increased parasitic capacitance in GPDK180 contribute to a slower response, but they also provide benefits such as improved noise tolerance and a more straightforward fabrication process. These factors make GPDK180 a more suitable choice for applications that do not require ultra-high speeds but instead focus on energy efficiency, reliability, and cost-effectiveness.

Ultimately, the choice between GPDK45 and GPDK180 depends on the specific requirements of the application. Selecting the appropriate technology node requires balancing the need for speed with considerations such as power consumption, design complexity, and overall cost. This trade-off underscores the importance of tailoring the technology selection to the unique demands of the intended circuit, ensuring optimal performance based on the desired specifications.

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